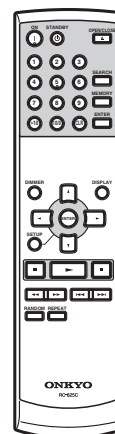


ONKYO SERVICE MANUAL

Ref. No. 3911
122005
/ 092006

COMPACT DISC PLAYER MODEL DX-7555




RC-625C

Black, Silver and Golden models

BMPP	230-240V AC, 50Hz
SMPP	230-240V AC, 50Hz
GMGT	220-230V AC, 50/60Hz
GMGR	220-230V AC, 50/60Hz
GMDT	120V AC, 60Hz
BMDC	120V AC, 60Hz
SMDC	120V AC, 60Hz

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK  ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

SPECIFICATIONS

Signal readout :	Optical non-contact
Frequency response :	2 Hz - 20 kHz
SN ratio :	111 dB
Audio dynamic range :	100 dB
THD (total harmonic distortion) :	0.0027%
Audio output	
Digital optical :	-22.5 dBm
Audio output / Impedance	
Digital coaxial :	0.5 V _{p-p} , 75 ohm
Audio output / Impedance	
Analog :	2.0 V (rms), 470 ohm
Power supply :	AC 230 - 240 V, 50 Hz AC 220 - 230 V, 50/60 Hz AC 120 V, 60 Hz
Power consumption :	16 W / 14 W
Standby power consumption :	European : 0.5 W North American : 0.3 W Others : 0.4 W / 0.3 W
Dimensions (W x H x D) :	435 x 111 x 405 mm
Weight :	8.0 kg
Operation condition	
Temperature, humidity :	5 - 35 °C, 5 - 85 % (no condensation)
Supported discs :	CD, CD-R, CD-RW, MP3 (Discs that have not been properly finalized may only be partially playable or not playable at all.)

Specifications and appearance are subject to change for improvement without prior notice.

SERVICE PROCEDURE-1

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs a laser. Therefore, be sure to follow carefully the instructions below when servicing.

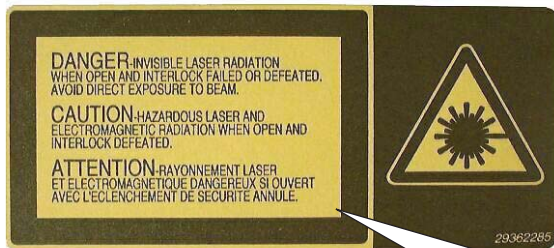
WARNING!!

SERVICE WARNING : DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION, BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICKUP BLOCK.

LASER WARNING LABEL

The labels shown below are affixed.

1. Warning label



DANGER:
INVISIBLE LASER RADIATION WHEN OPEN AND INTERLOCK FAILED OR DEFEATED. AVOID DIRECT EXPOSURE TO BEAM.

CAUTION:
HAZARDOUS LASER AND ELECTROMAGNETIC RADIATION WHEN OPEN AND INTERLOCK DEFEATED.

ATTENTION:
RAYONNEMENT LASER ET ELECTROMAGNETIQUE DANGEREUX SI OUVERT AVEC L'ECLANCHEMENT DE SECURITE ANNULE.

2. Class 1 label



LUOKAN 1
LASERLAITE
KLASS 1
LASER APPARAT

Printed on rear panel

PRECAUTIONS

1. Ground for the work-desk.
Place a conductive sheet such as a sheet of copper (with impedance lower than 10 Mohm) on the work-desk and place the set on the conductive sheet so that the chassis can be grounded.
2. Grounding for the test equipments and tools.
Test equipments and toolings should be grounded in order that their ground level is the same the ground of the power source.
3. Grounding for the human body.
Be sure to put on a wrist-strap for grounding whose other end is grounded.
Be particularly careful when the workers wear synthetic fiber clothes, or air is dry.
4. Select a soldering iron that permits no leakage and have the tip of the iron well-grounded.
5. Do not check the laser diode terminals with the probe of a circuit tester or oscilloscope.

SERVICE PROCEDURE-2

1. Initialize the unit.

- (1) Press and hold down the STOP [■] button, then press the FF (fast forward) [▶▶] button. All segments light up.
- (2) Press and hold down the STOP [■] button, then press the PUSH TO ENTER (JOG) button.

FL display 0 0:00 ---> NO DISC

- (3) Press the POWER button to turn off the unit.
- (4) Disconnect the AC power cord from a wall outlet.

2. Check the version of Main microprocessor (Q8005) and Servo microprocessor (Q1001).

- (1) Connect the AC power cord into a wall outlet.
- (2) Press the POWER button to turn on the unit.
- (3) Change into the state of "NO DISC".
- (4) Press and hold down the STOP [■] button, then press the FF (fast forward) [▶▶] button twice.
The first press lights up all segments.

Main microprocessor version ---> Servo microprocessor version

FL display MA 050830A ---> SRV 5805A ---> MODEL00 00 ---> NO DISC

- (5) Press the POWER button to turn off the unit.
- (6) Disconnect the AC power cord from a wall outlet.

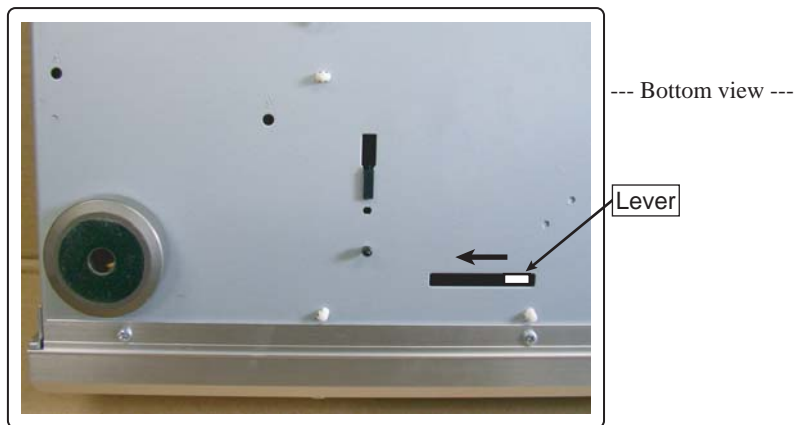
3. Setting position before shipment.

- (1) POWER button : OFF
- (2) PHONES LEVEL : MIN.

4. Take out the Disc.

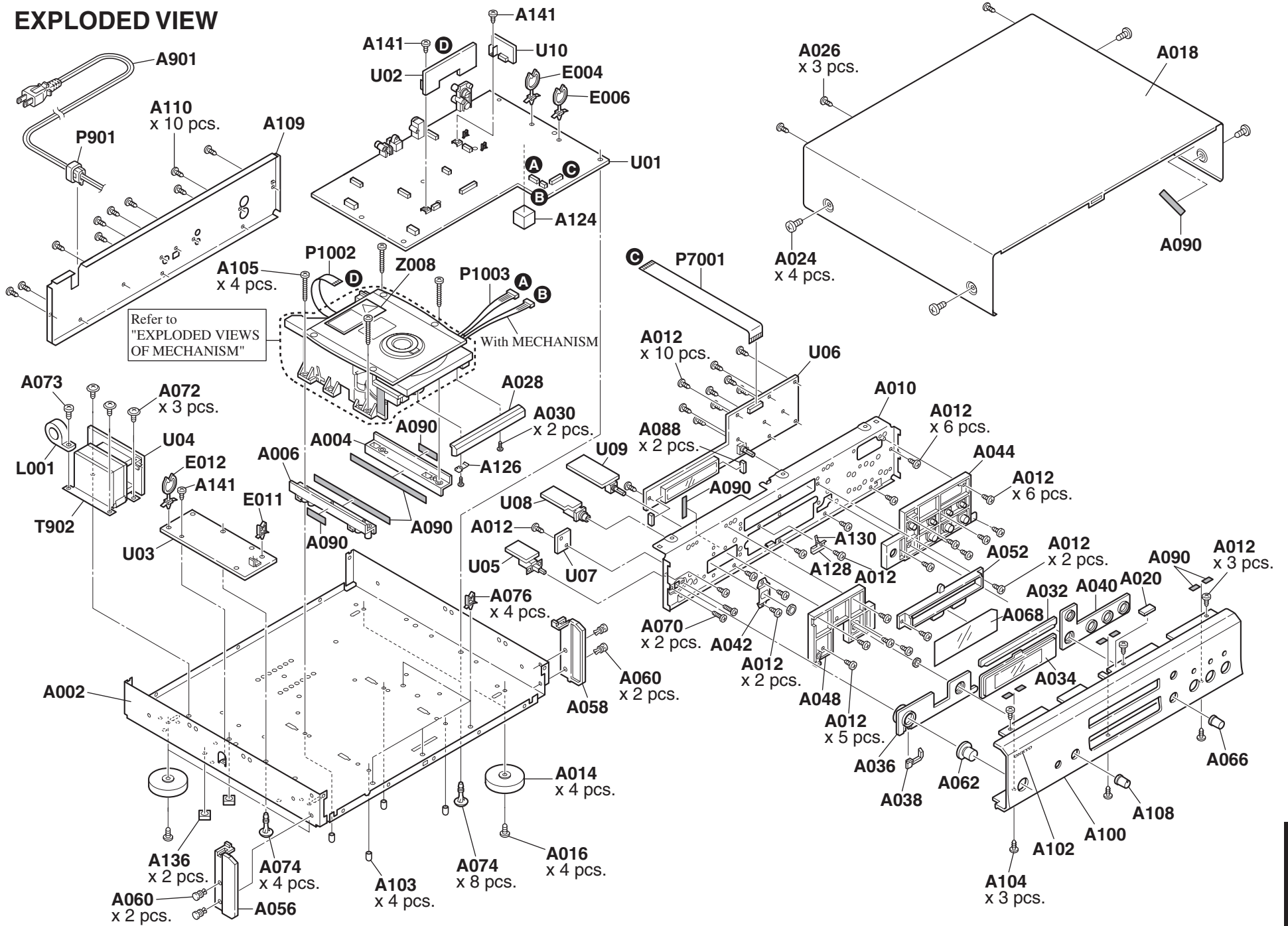
If cannot take out the disc, please take out disc as follows.

- (1) The lever in the direction of the arrow.
- (2) The tray is slowly drawn out by the hand.



Front panel

EXPLODED VIEW



EXPLODED VIEWS OF MECHANISM-1

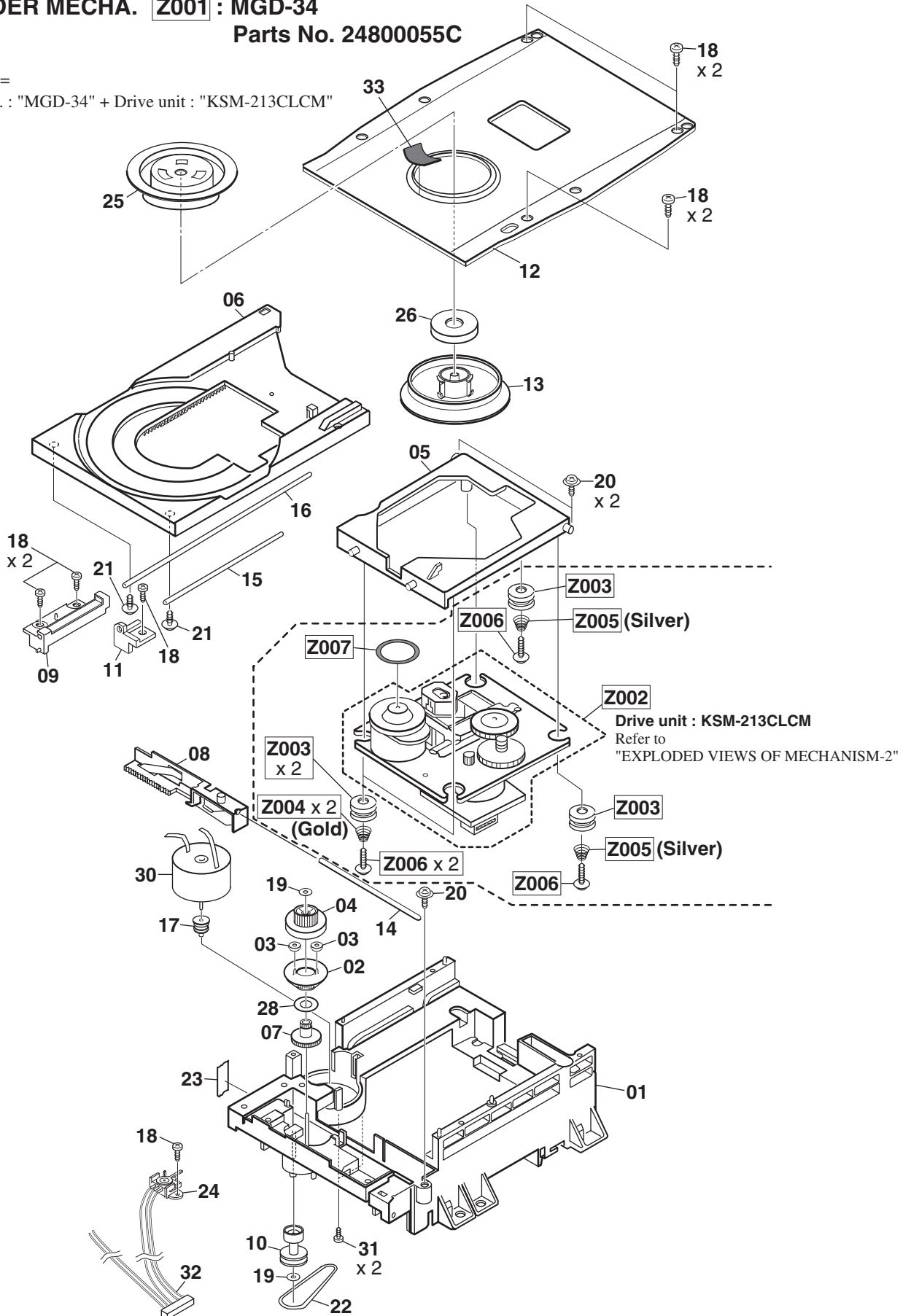
CD LOADER MECHA. [Z001] : MGD-34

Parts No. 24800055C

<Note>

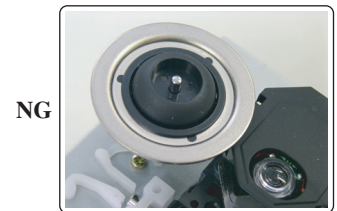
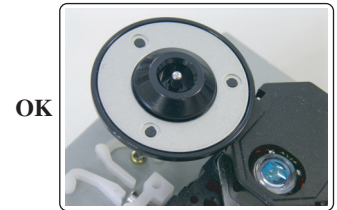
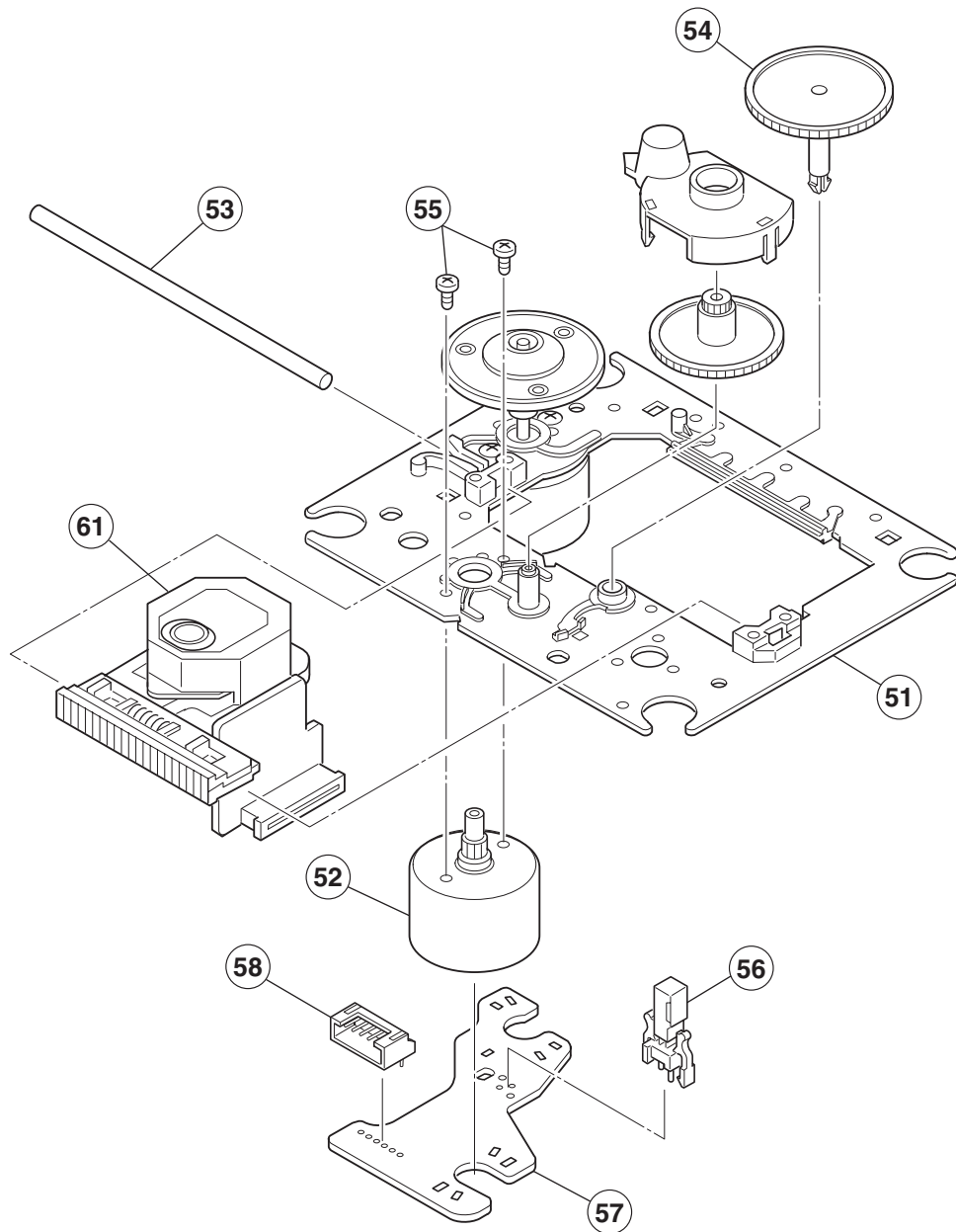
CD MECHA. =

Loader mecha. : "MGD-34" + Drive unit : "KSM-213CLCM"



EXPLODED VIEWS OF MECHANISM-2

CD DRIVE UNIT : KSM-213CLCM







PARTS LIST

REF. NO.	PART NO. (SN)	DESCRIPTION	Q'TY
51	X-2625-877-1	Motor chassis ass'y	1
52	X2625-769-1	Motor gear ass'y	1
53	2626-908-01	Sled shaft	1
54	24810023	Gear (A) (S)	1
55	7621-255-15	P2 x 3, Screw	2
56	24840008	Leaf switch	1
57	1639-678-12	Motor PC board	1
58	1-564-722-11	Connector 6pin	1
61	8848-483-05	KSS-213C, Pickup	1

SCHEMATIC DIAGRAMS-1

U01 : MAIN CIRCUIT PC BOARD NAAR-8645

NOTE

- THE COMPONENTS IDENTIFIED BY MARK  ARE CRITICAL FOR SAFETY. REPLACE ONLY WITH PART NUMBER SPECIFIED.
- VOLTAGE (MEASURED WITH VOLTMETER)  IS DC VOLTAGE. (NO INPUT SIGNAL)
- ELECTROLYTIC CAPACITORS () ARE IN uF/WV.
- ALL CAPACITORS ARE IN pF/50V UNLESS OTHERWISE NOTED.
EX) 030 +3pF 330 +33pF 331+330pF 333+0.03uF
- ALL RESISTORS ARE IN OHMS 1/4WATTS UNLESS OTHERWISE NOTED.
THE THICK LINES ON PC BOARD ARE THE PRINTING SIDE OF THE PARTS.
EX)  PRINTING SIDE
- CIRCUIT IS SUBJECT TO CHANGE FOR IMPROVEMENT.

CAUTION

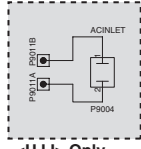


FOR CONTINUED PROTECTION AGAINST FIRE HAZARD, REPLACE ONLY WITH FUSE OF SAME TYPE AND RATING INDICATED.

ATTENTION

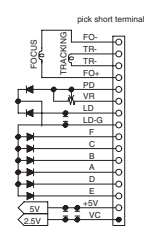
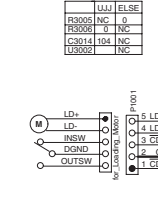
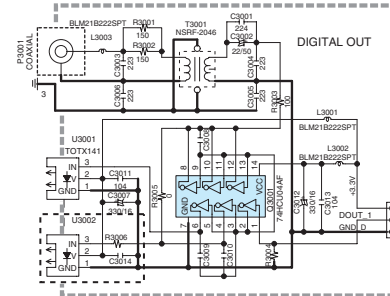


AFIN D'ASSURER UNE PROTECTION PERMANENTE CONTRE LES RISQUES D'INCENDIE, REPLACER UNIQUEMENT PAR UN FUSIBLE DE MEME TYPE ET CALIBRATION COMME INDIQUE.

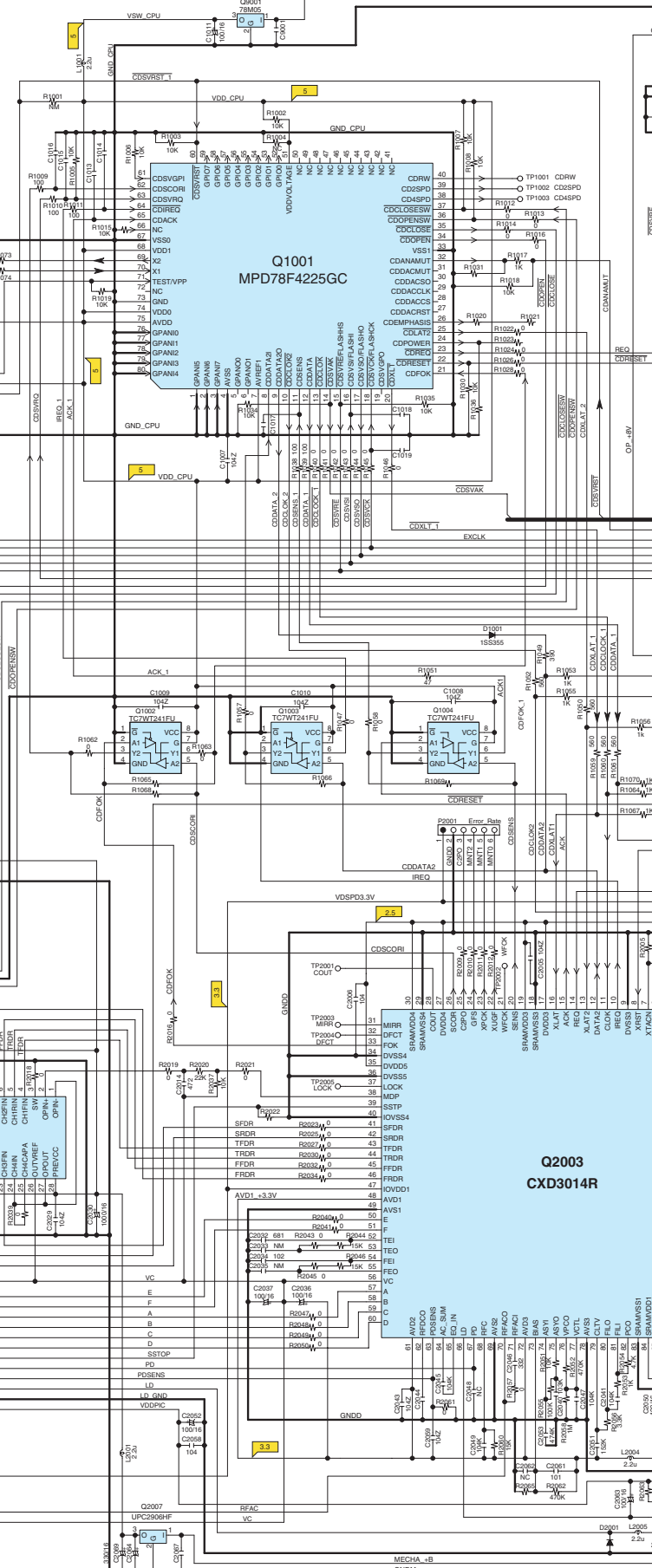
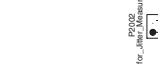
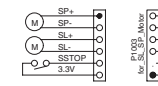


<UJ> Only

NC	2	FLASHHS	R1025	0	CDSVRE
Vsp/test	3	FLASH VPI	R1026	0	FLASHVPI
EVSV	4	FLASHRS	R1029	0	CDSVRS
RST	5	FLASHCK	R1030	0	CDSVCK
CDSVCK	6	FLASHQ	R1031	0	CDSVQ
CDSVSO	7	FLASHI	R1032	0	CDSVSI
CPUGND	8				



U02 : CONNECTOR PC BOARD NAETC-8736



Q2003 CXD3014R

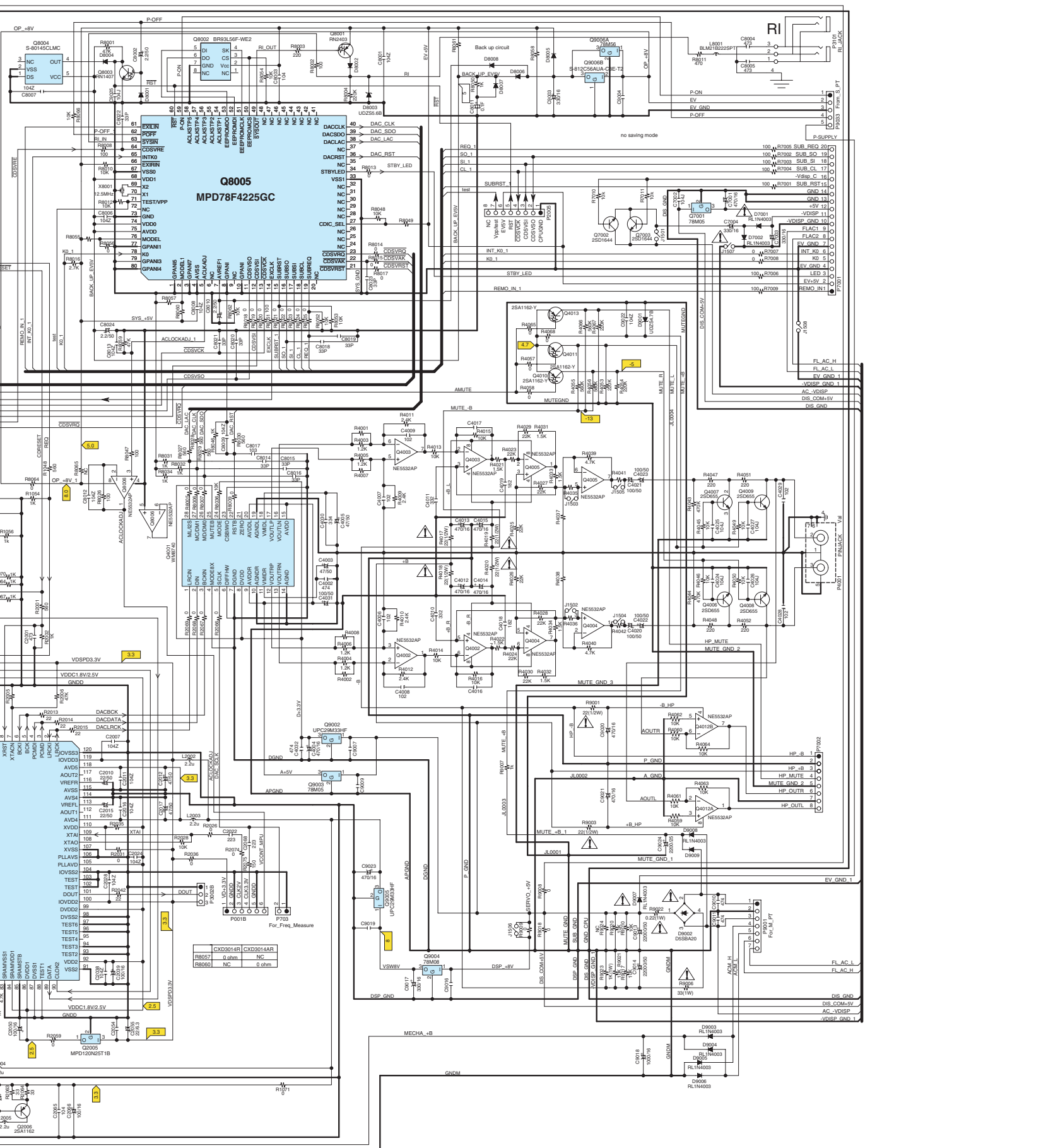
1

2

3

4

5

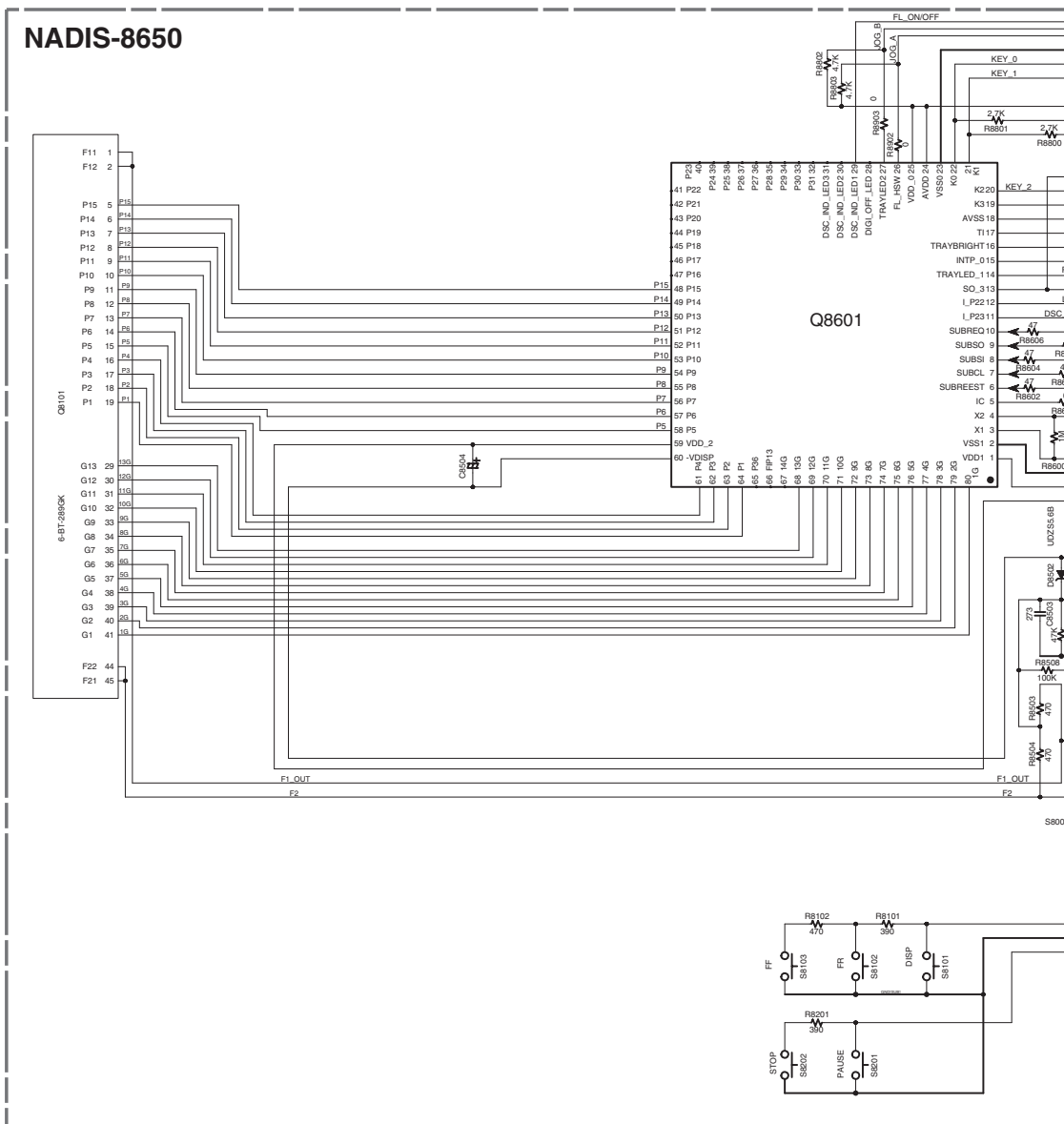


A B C D
SCHEMATIC DIAGRAMS-2 U06 : DISPLAY CIRCUIT PC BOARD NADIS-8650

1

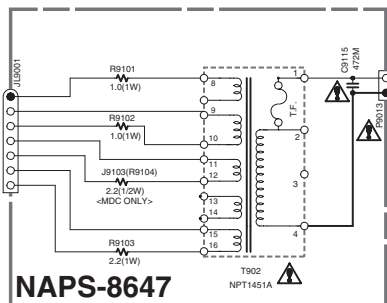
2

3

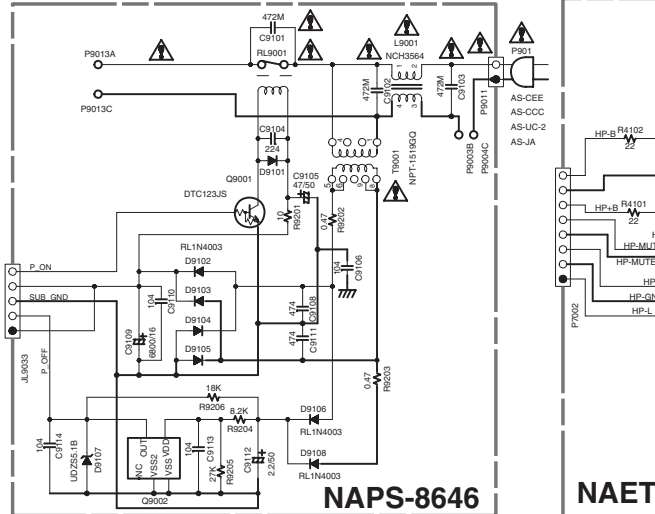


4

U04 : POWER TRANSFORMER PC BOARD NAPS-8647

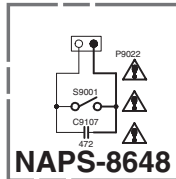


U03 : POWER SUPPLY CIRCUIT PC BOARD NAPS-8646

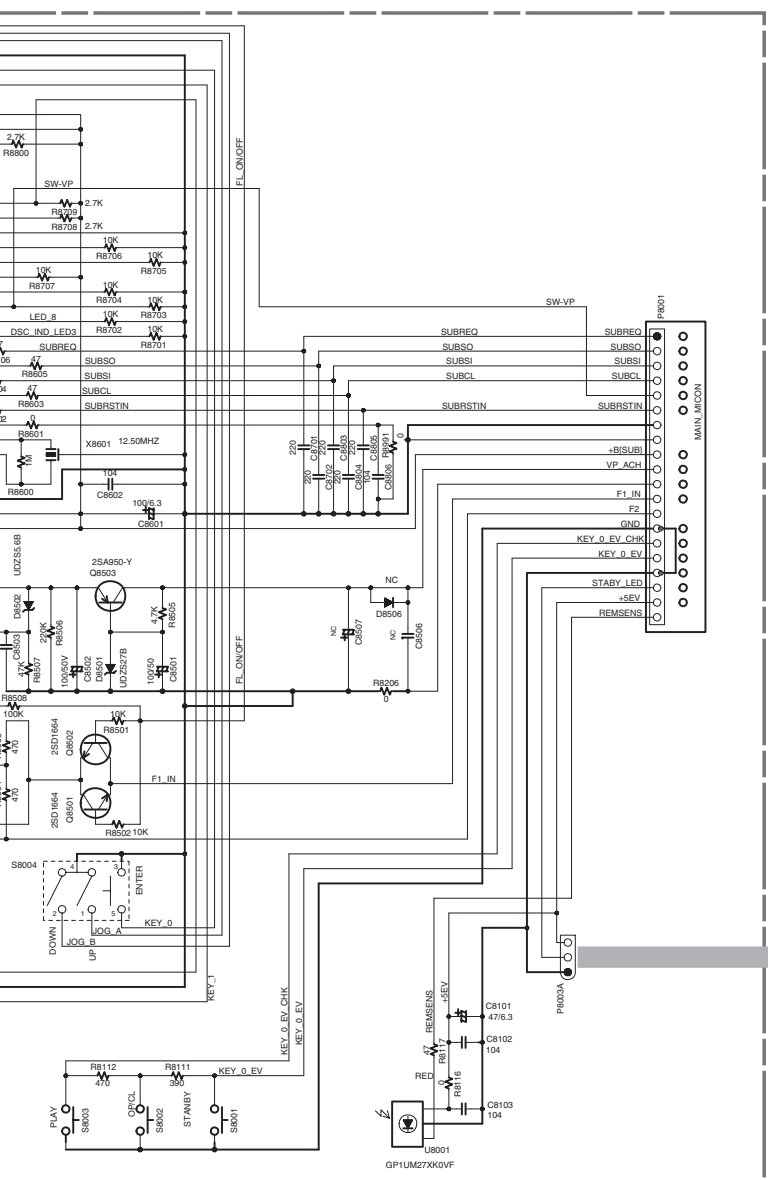


5

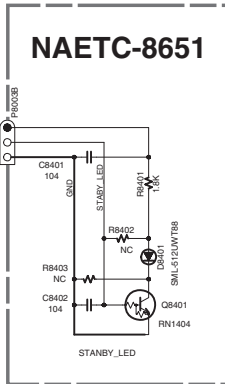
U05 : POWER SWITCH PC BOARD NAPS-8648



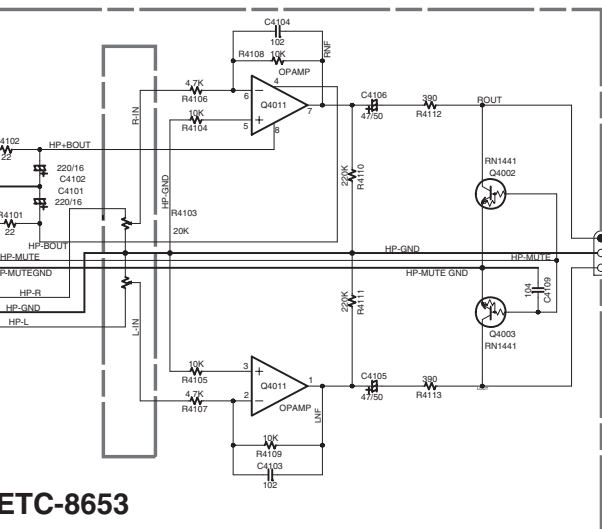
NAET



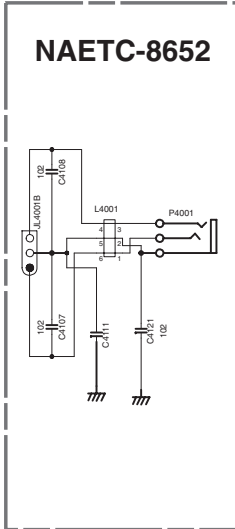
**U07 : STANDBY LED PC BOARD
NAETC-8651**



**U09 : HEADPHONE AMP. PC BOARD
NAETC-8653**



**U08 : HEADPHONE JACK PC BOARD
NAETC-8652**



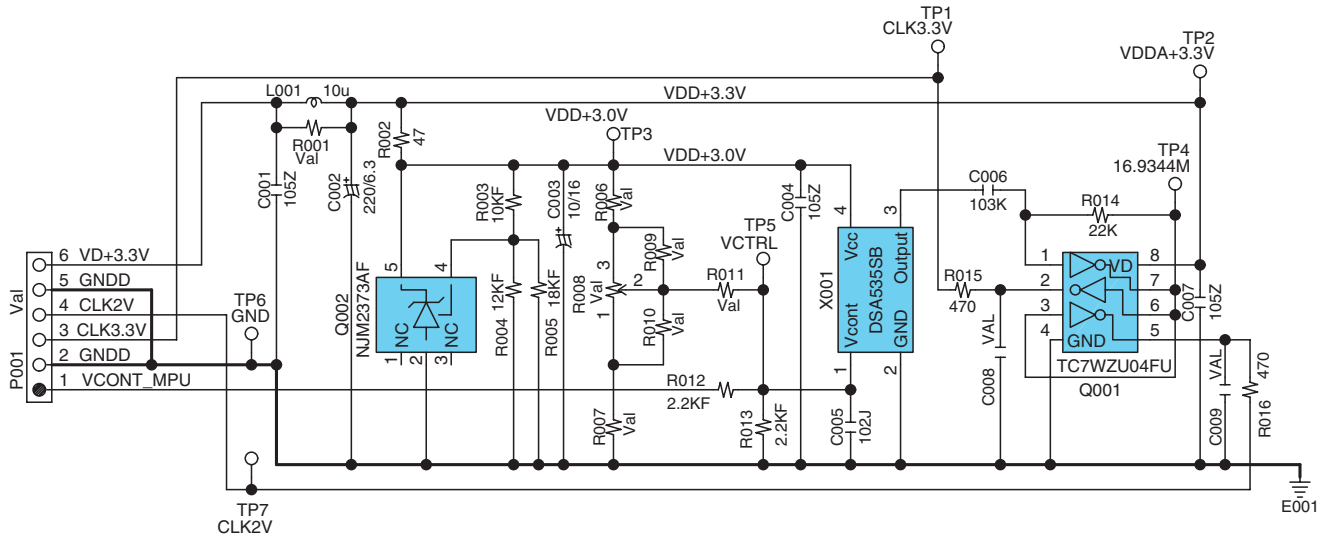
A B C D E

SCHEMATIC DIAGRAMS-3

1

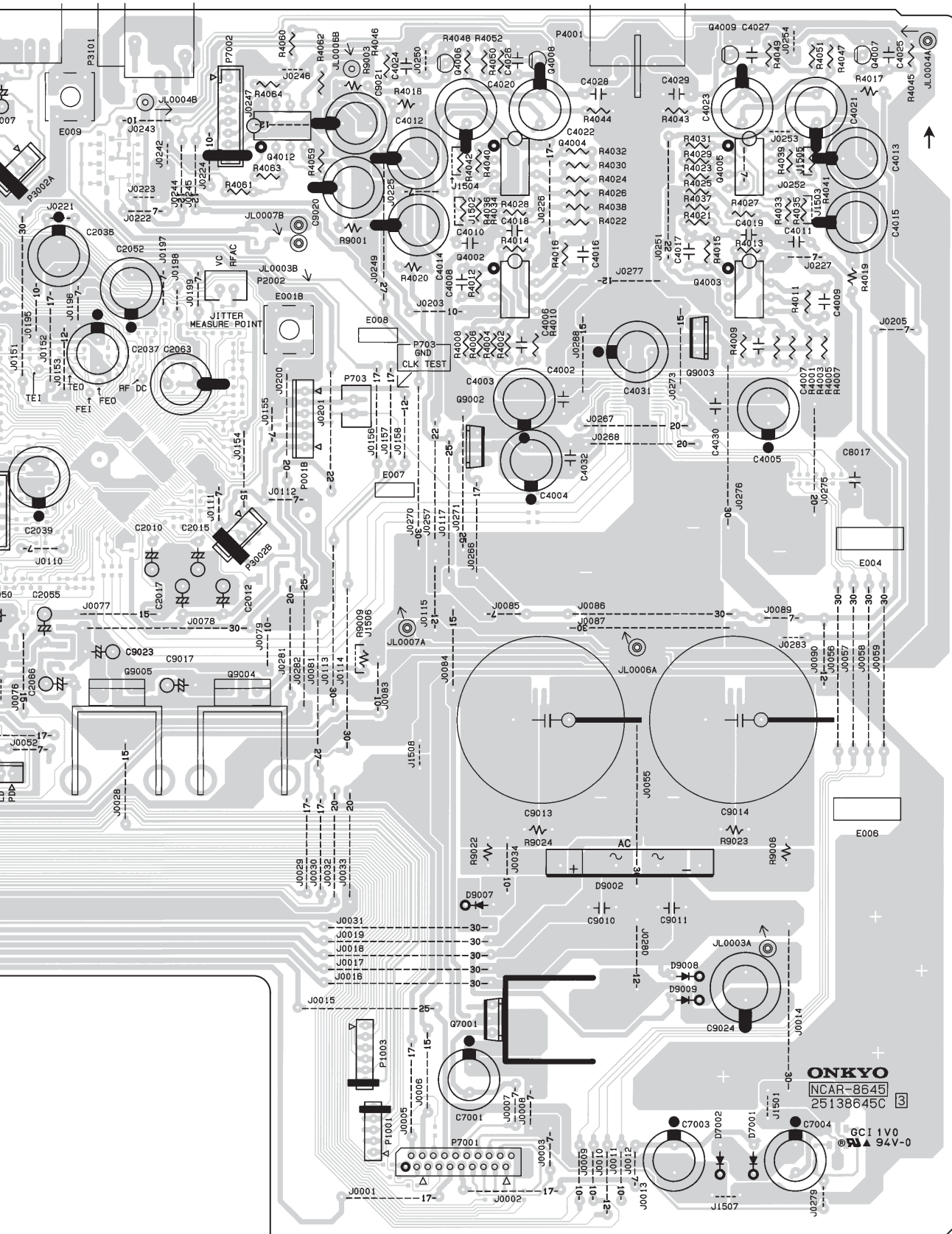
U10 : SUPER PRECISION CLOCK PC BOARD NADG-8725

2



3

4



ONKYO
NCAR-8645
25138645C

GCI 1V0
94V-0

A

B

C

D

PRINTED CIRCUIT BOARD VIEWS-2

U01 MAIN CIRCUIT PC BOARD (NAAR-8645)

Soldering side

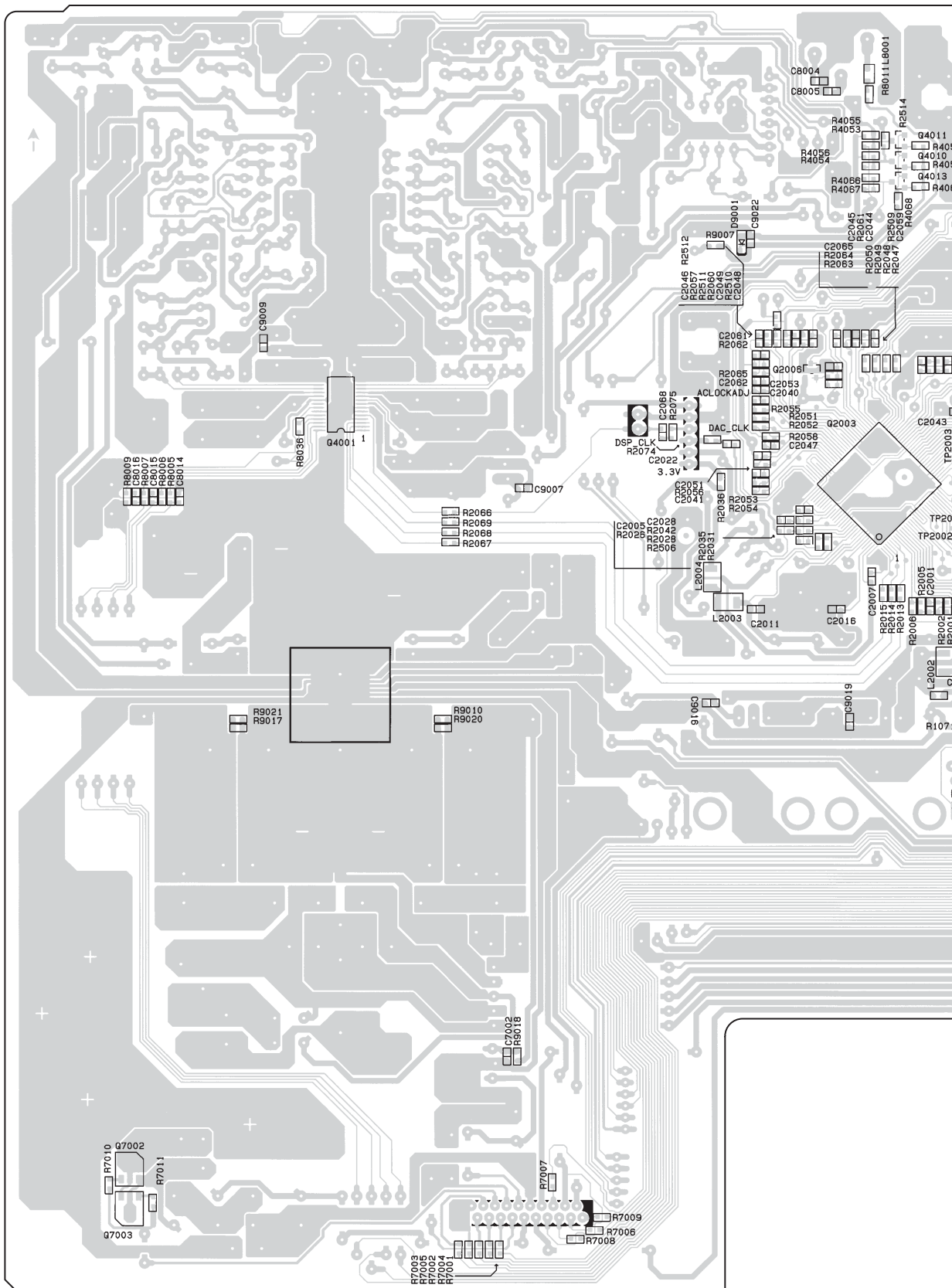
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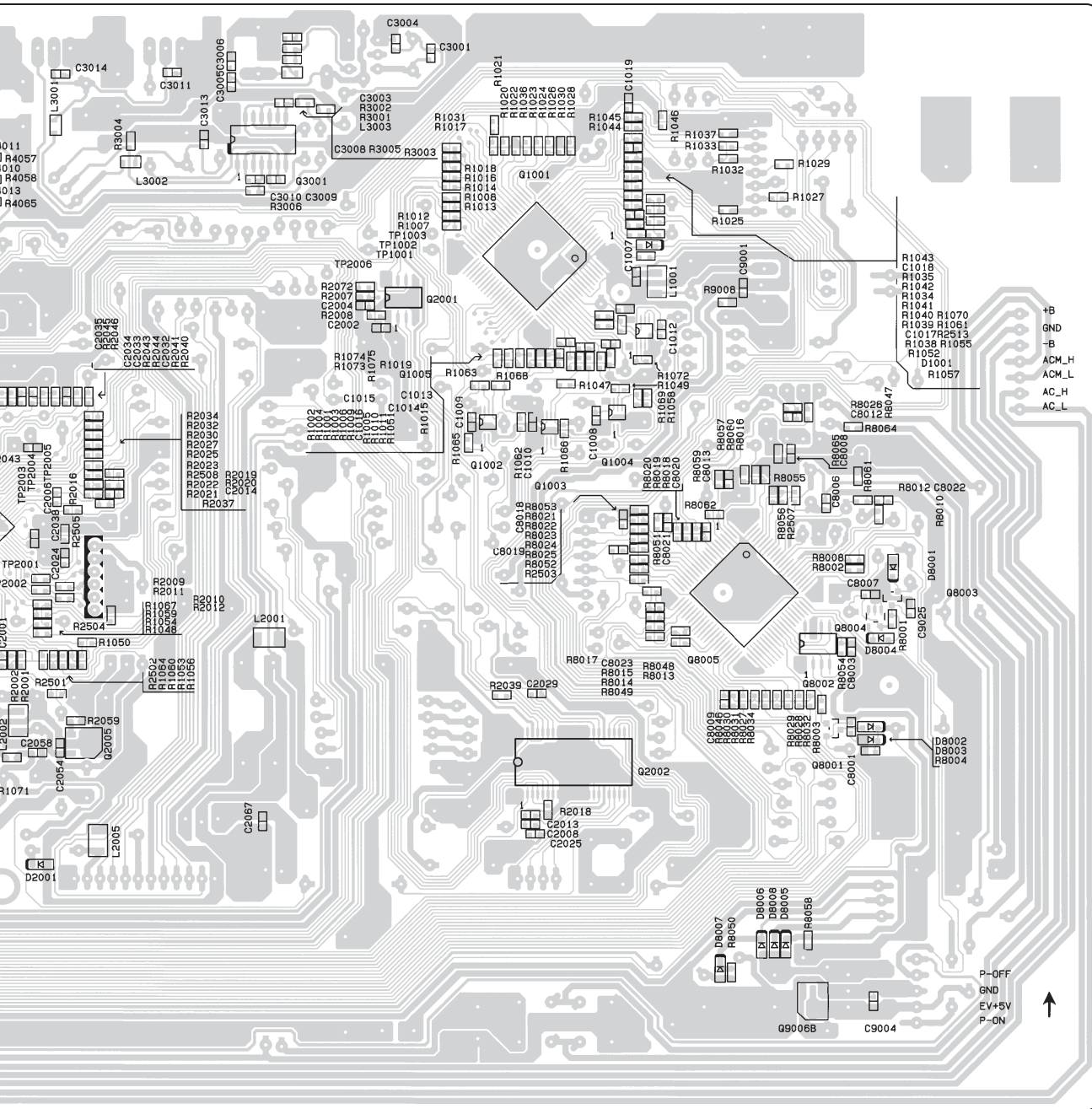
2

3

4

5





A

B

C

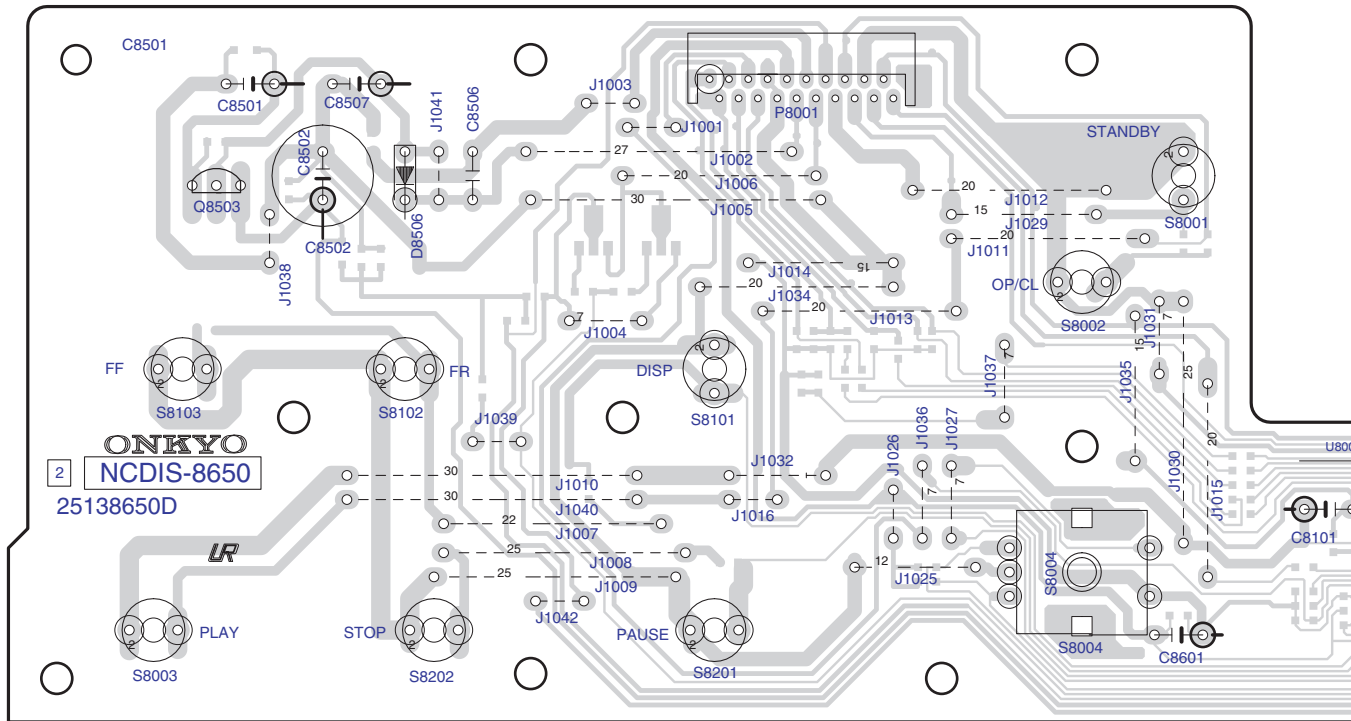
D

PRINTED CIRCUIT BOARD VIEWS-3
(FROM SOLDERING SIDE)

1

U06 DISPLAY CIRCUIT PC BOARD (NADIS-8650)

Component side

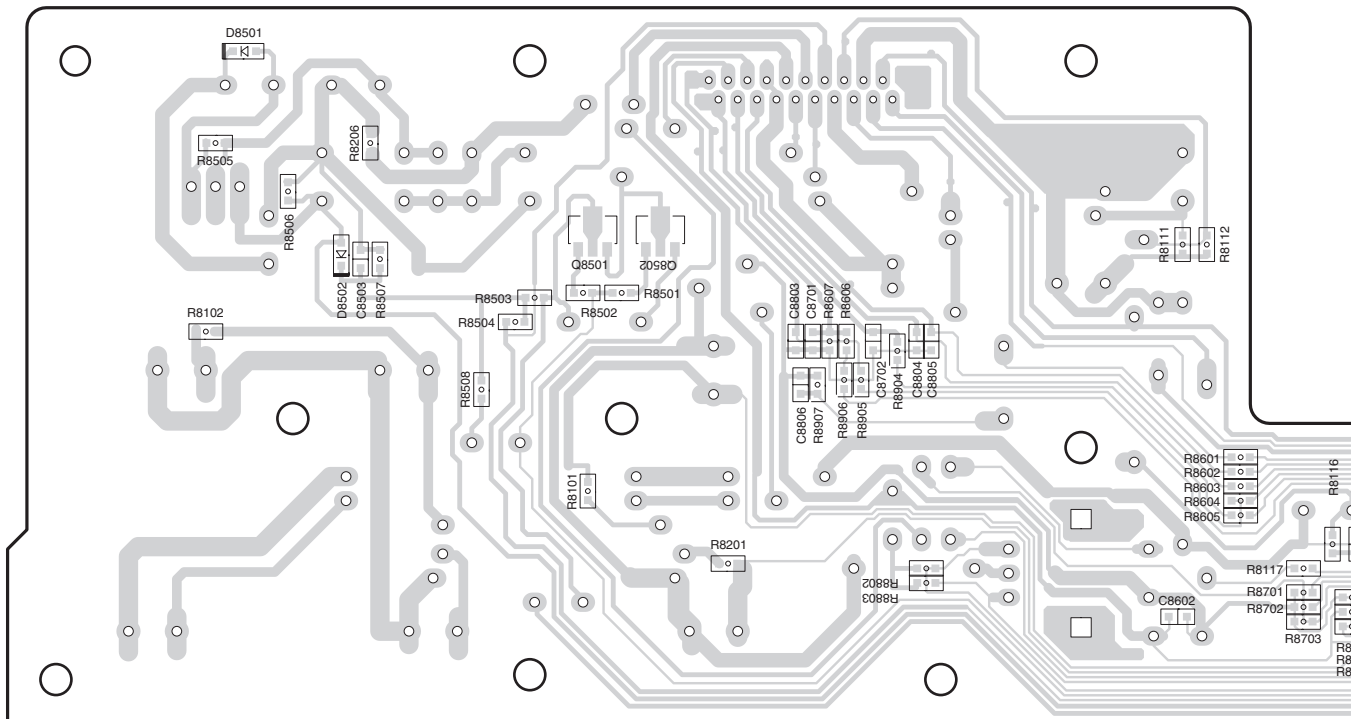


2

3

4

Soldering side



5

E

F

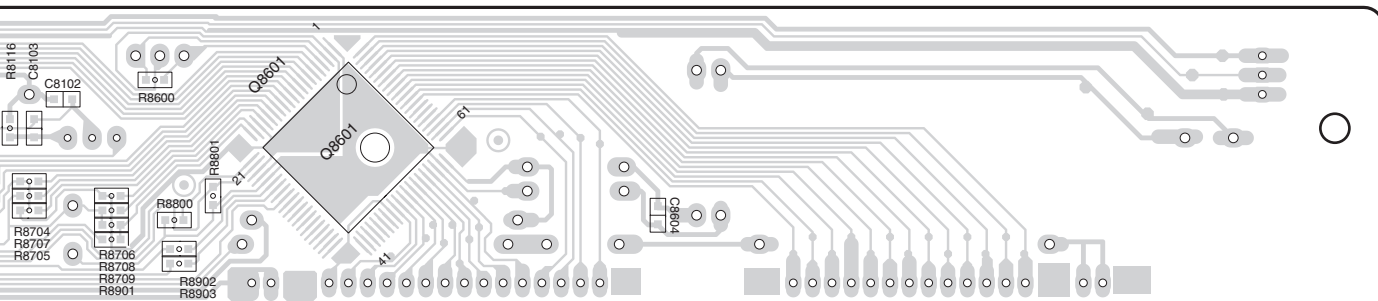
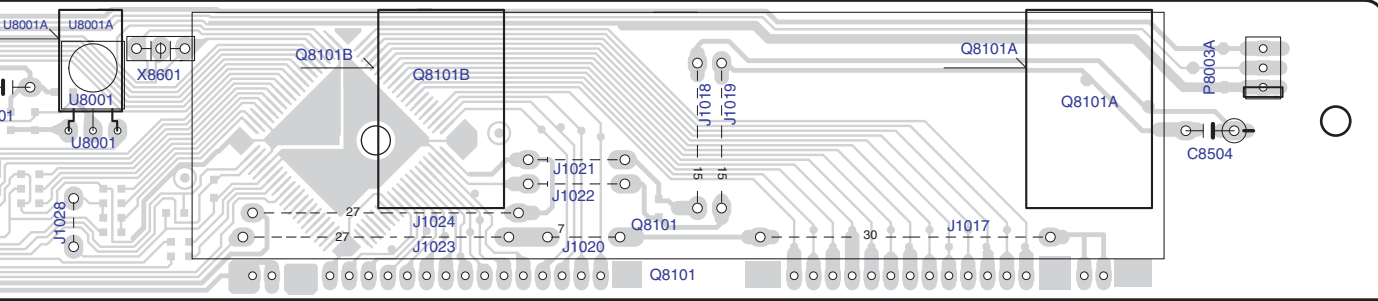
G

H

U10 SUPER PRECISION CLOCK PC BOARD (NADG-8725)

No PC board view.

Look over the actual PC board on hand.



A

B

C

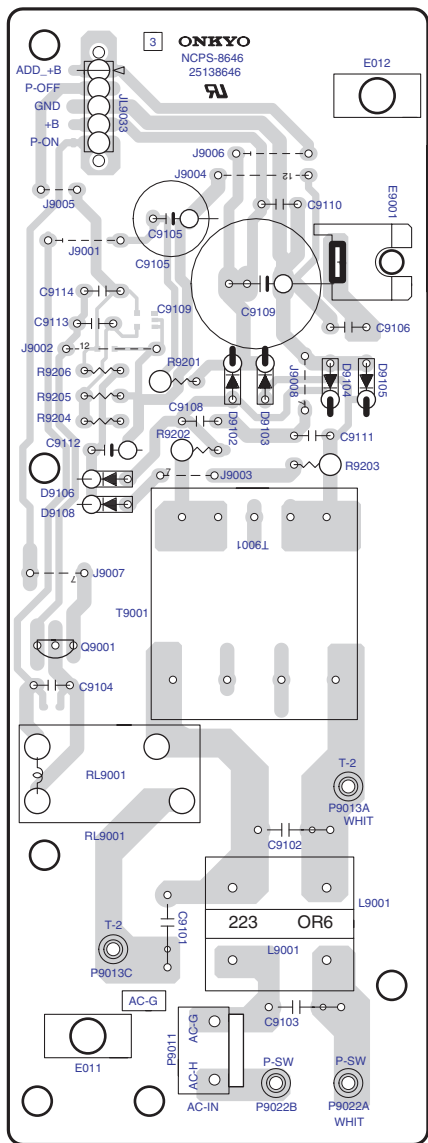
D

PRINTED CIRCUIT BOARD VIEWS-4

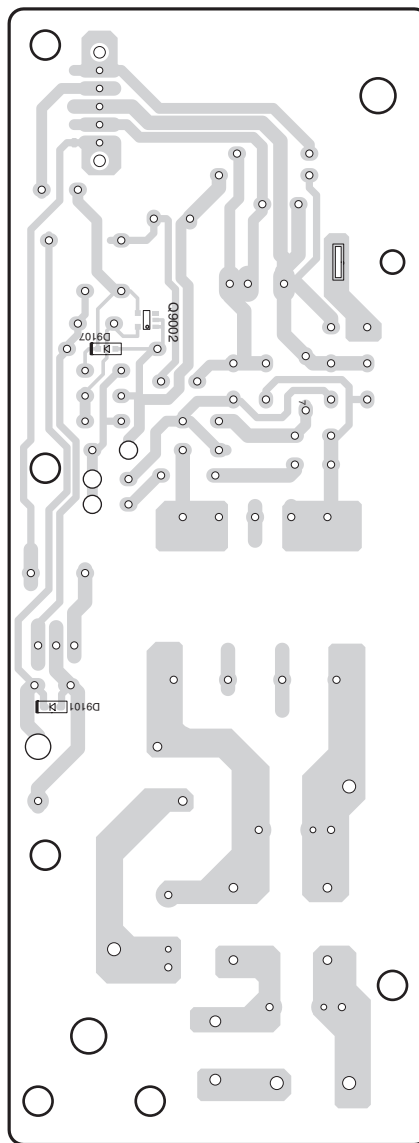
(FROM SOLDERING SIDE)

U03 POWER SUPPLY CIRCUIT PC BOARD (NAPS-8646)

1



Component side



Soldering side

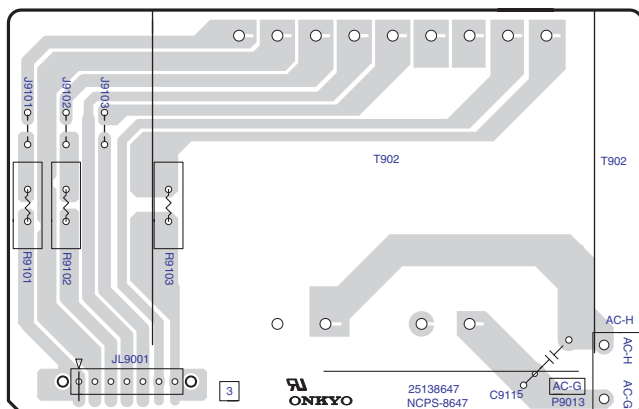
2

3

4

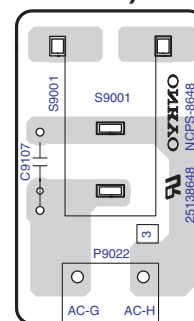
U04 POWER TRANSFORMER PC BOARD (NAPS-8647)

5



Component side

U05 POWER SWITCH PC BOARD (NAPS-8648)



Component side

A

B

C

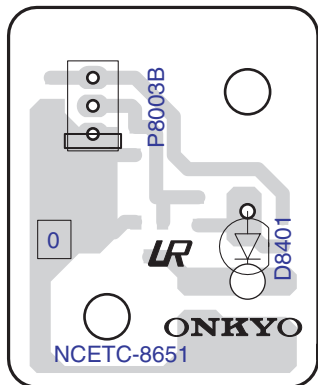
D

PRINTED CIRCUIT BOARD VIEWS-5

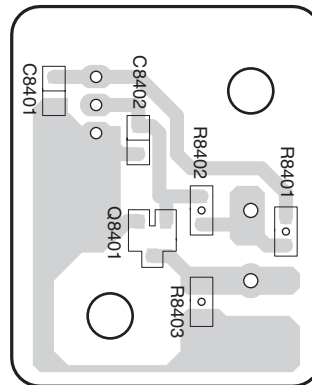
(FROM SOLDERING SIDE)

1

U07 STANDBY LED PC BOARD (NAETC-8651)



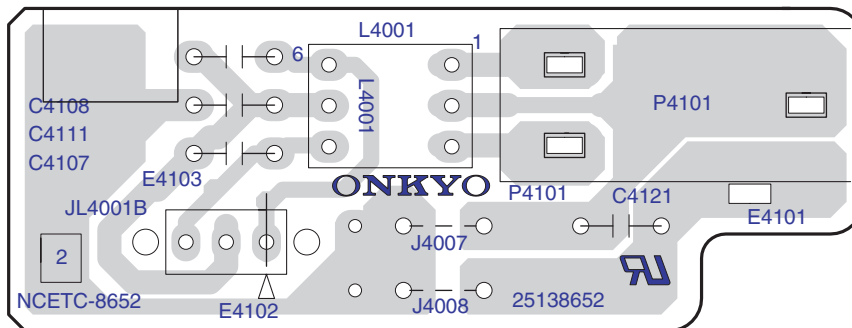
Component side



Soldering side

2

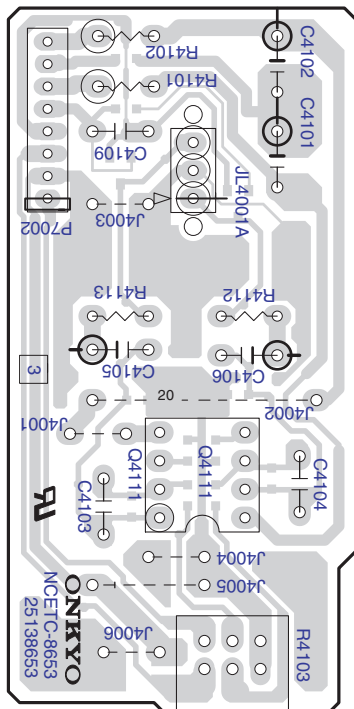
U08 HEADPHONE JACK PC BOARD (NAETC-8652)



Component side

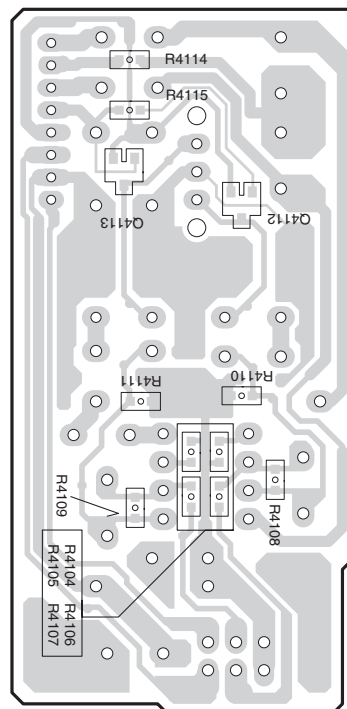
3

U09 HEADPHONE AMP. PC BOARD (NAETC-8653)



Component side

4



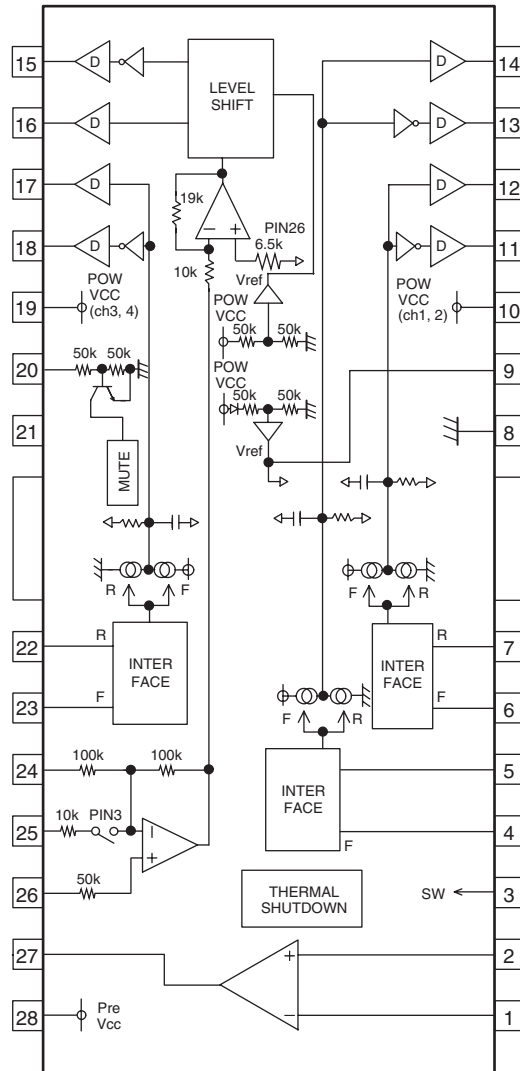
Soldering side

5

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-1

Q2002 : BA5947FP (4-ch BTL DRIVER)

BLOCK DIAGRAM



TERMINAL DESCRIPTION

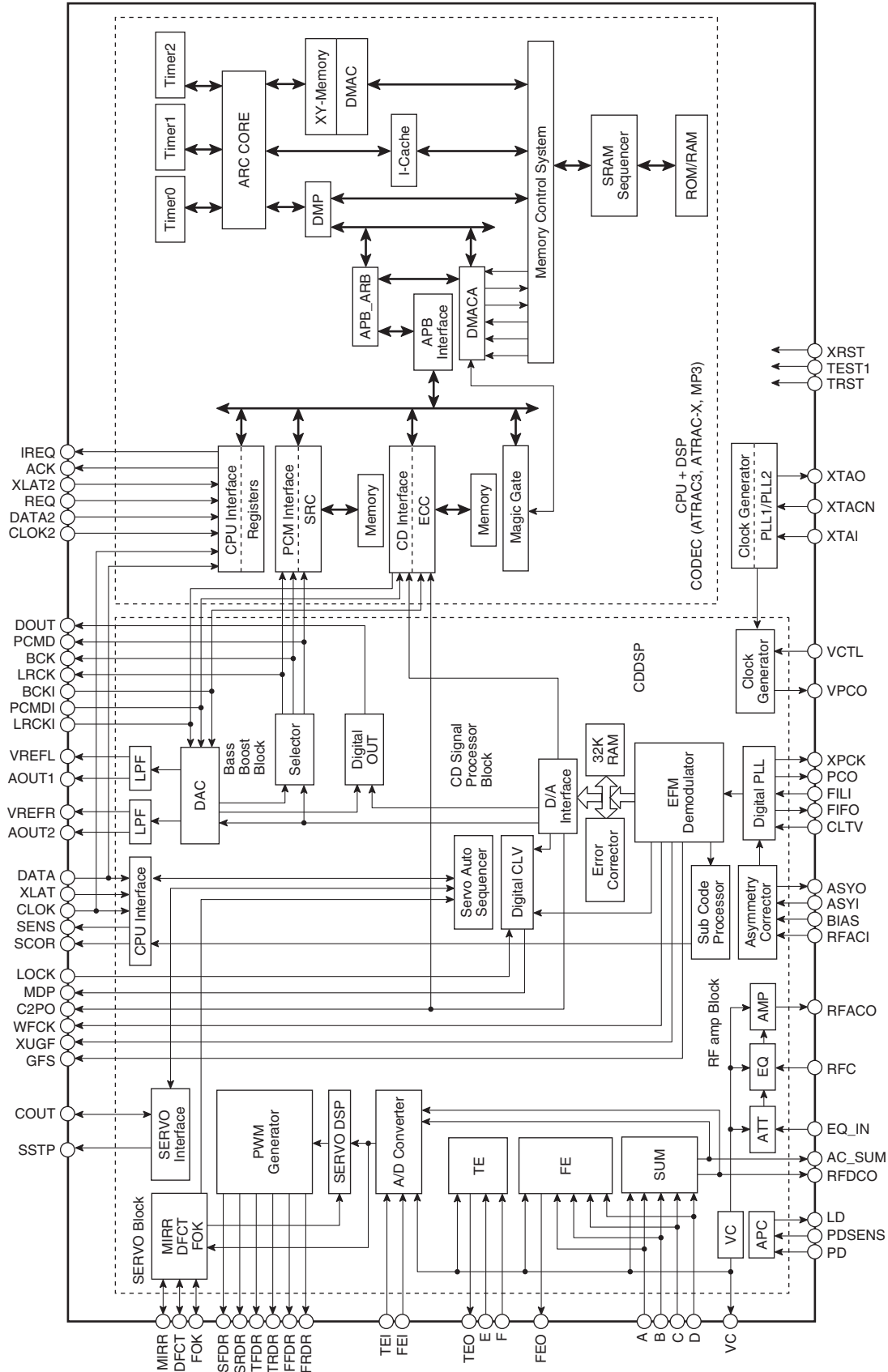
No.	PIN NAME	DESCRIPTION
1	OPIN-	Operational amplifier negative input terminal
2	OPIN+	Operational amplifier positive input terminal
3	SW	CH4 input selecting switch terminal
4	CH1FIN	CH1 PWM forward input terminal
5	CH1RIN	CH1 PWM reverse input terminal
6	CH2FIN	CH2 PWM forward input terminal
7	CH2RIN	CH2 PWM reverse input terminal
8	GND	GND
9	VREFIN	Internal Vref voltage input terminal
10	POWVCC	Power part power supply voltage (CH1, 2)
11	CH2OUTR	CH2 reverse output terminal
12	CH2OUTF	CH2 forward output terminal
13	CH1OUTR	CH1 reverse output terminal
14	CH1OUTF	CH1 forward output terminal

No.	PIN NAME	DESCRIPTION
15	CH4OUTR	CH4 reverse output terminal
16	CH4OUTF	CH4 forward output terminal
17	CH3OUTF	CH3 forward output terminal
18	CH3OUTR	CH3 reverse output terminal
19	POWVCC	Power part power supply voltage (CH3, 4)
20	MUTE	Mute terminal
21	GND	GND
22	CH3RIN	CH3 PWM reverse input terminal
23	CH3FIN	CH3 PWM forward input terminal
24	CH4IN	CH4 input terminal
25	CH4CAPA	CH4 external CAPA connection terminal
26	OUTVREF	CH4 external reference voltage input terminal
27	OPOUT	Operational amplifier output terminal
28	PREVCC	Pre-part power supply voltage

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-2

Q2003 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -1/4

BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-3

Q2003 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -2/4

TERMINAL DESCRIPTION

Pin No.	Pin name	I/O	Description
1	LRCK	O	LR clock output.
2	LRCKI	I	LR clock input.
3	PCMD	O	PCMD data output.
4	PCMDI	I	PCMD data input.
5	BCK	O	BCK data output.
6	BCKI	I	BCK data input.
7	XTACN	I	Oscillation circuit control. Self-oscillation when high, oscillation stop when low.
8	XRST	I	System reset. Reset when low.
9	DVss3	---	Internal digital GND.
10	IREQ	O	ARC → Interrupt to microprocessor.
11	CLOK	I	CPU I/F ARC(CLK)
12	DATA2	I/O	CPU I/F ARC(DATA)
13	XLAT2	I	Codec latch signal.
14	REQ	I	CPU I/F ARC (REQ).
15	ACK	O	CPU I/F ARC (ACK).
16	XLAT	I	CDDSP control latch signal.
17	DVDD3	---	Internal digital power supply.
18	DVss8	---	Internal digital GND.
19	DVDD8	---	Internal digital power supply.
20	SENS	O	SENS output to CPU.
21	WFCK	O	WFCK output.
22	XUGF	O	XUGF output. Output MNT0, RFCK, SOUT by command switch.
23	XPCK	O	XPCK output. Output MNT1, SOCK by command switch.
24	GFS	O	GFS output. Output MNT2, XROF, XOLT by command switch.
25	C2PO	O	C2PO output. Output MNT3, GTOP by command switch.
26	SCOR	O	High output when the subcode sync, S0 or S1, is detected.
27	DVDD4	---	Digital power supply.
28	COUT	I/O	Track number count signal input/output.
29	DVss9	---	Internal digital GND.
30	DVDD9	---	Internal digital power supply.
31	MIRR	I/O	Mirror signal input/output.
32	DFCT	I/O	Defect signal input/output.
33	FOK	I/O	Focus OK signal input/output.
34	DVss4	---	Internal digital GND.
35	DVDD5	---	Internal digital power supply.
36	DVss5	---	Internal digital GND.
37	LOCK	I/O	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Or input when LKIN = "1".
38	MDP	O	Spindle motor servo control output.
39	SSTP	I	Disc innermost detection signal input.
40	IOVss1	---	I/O digital GND.
41	SFDR	O	Sled drive output.
42	SRDR	O	Sled drive output.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-4

Q2003 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -3/4

TERMINAL DESCRIPTION (Continued)

Pin No.	Pin name	I/O	Description
43	TFDR	O	Tracking drive output.
44	TRDR	O	Tracking drive output.
45	FFDR	O	Focus drive output.
46	FRDR	O	Focus drive output.
47	IOVDD1	---	I/O digital power supply.
48	AVD1	---	Analog power supply.
49	AVS1	---	Analog GND.
50	E	I	E signal input.
51	F	I	F signal input.
52	TEI	I	Tracking error signal input to DSSP block or F input.
53	TEO	O	Tracking error signal output from RF amplifier block.
54	FEI	I	Focus error signal input to DSSP block or A input.
55	FEO	O	Focus error signal output form RF amplifier block.
56	VC	I/O	Center voltage output from RF amplifier block. Center voltage input to DSSP block by command switch.
57	A	I	A signal input.
58	B	I	B signal input.
59	C	I	C signal input.
60	D	I	D signal input.
61	AVD2	---	Analog power supply.
62	RFDCO	I/O	RFDC signal output. RFDC signal input to DSSP block by command switch.
63	PDSSENS	I	Reference voltage pin for PD.
64	AC_SUM	O	RFAC summing amplifier output.
65	EQ_IN	I	Equalizer circuit input.
66	LD	O	APC amplifier output.
67	PD	I	APC amplifier input.
68	RFC	I	Equalizer cut-off frequency adjustment pin.
69	AVS2	---	Analog GND.
70	RFACO	O	RFAC signal output.
71	RFACI	I	RFAC signal input or EFM signal input.
72	AVD3	---	Analog power supply.
73	BIAS	I	Asymmetry circuit constant current input.
74	ASYI	I	Asymmetry comparator voltage input.
75	ASYO	O	EFM full-swing output. (Low = VSS, High = VDD)
76	VPCO	O	Wide-band EFM PLL charge pump output.
77	VCTL	I	Wide-band EFM PLL VCO2 control voltage input.
78	AVS3	---	Analog GND.
79	CLTV	I	Multiplier VCO1 control voltage input.
80	FILO	O	Master PLL (slave = digital PLL) filter output.
81	FILI	I	Master PLL filter input.
82	PCO	O	Master PLL charge pump output.
83	DVSS6	---	Internal digital GND.
84	DVDD6	---	Internal digital power supply.
85	SRAMSTB	I	Normally low.
86	DVDD1	---	Internal digital power supply.
87	DVSS1	---	Internal digital GND.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-5

Q2003 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -4/4

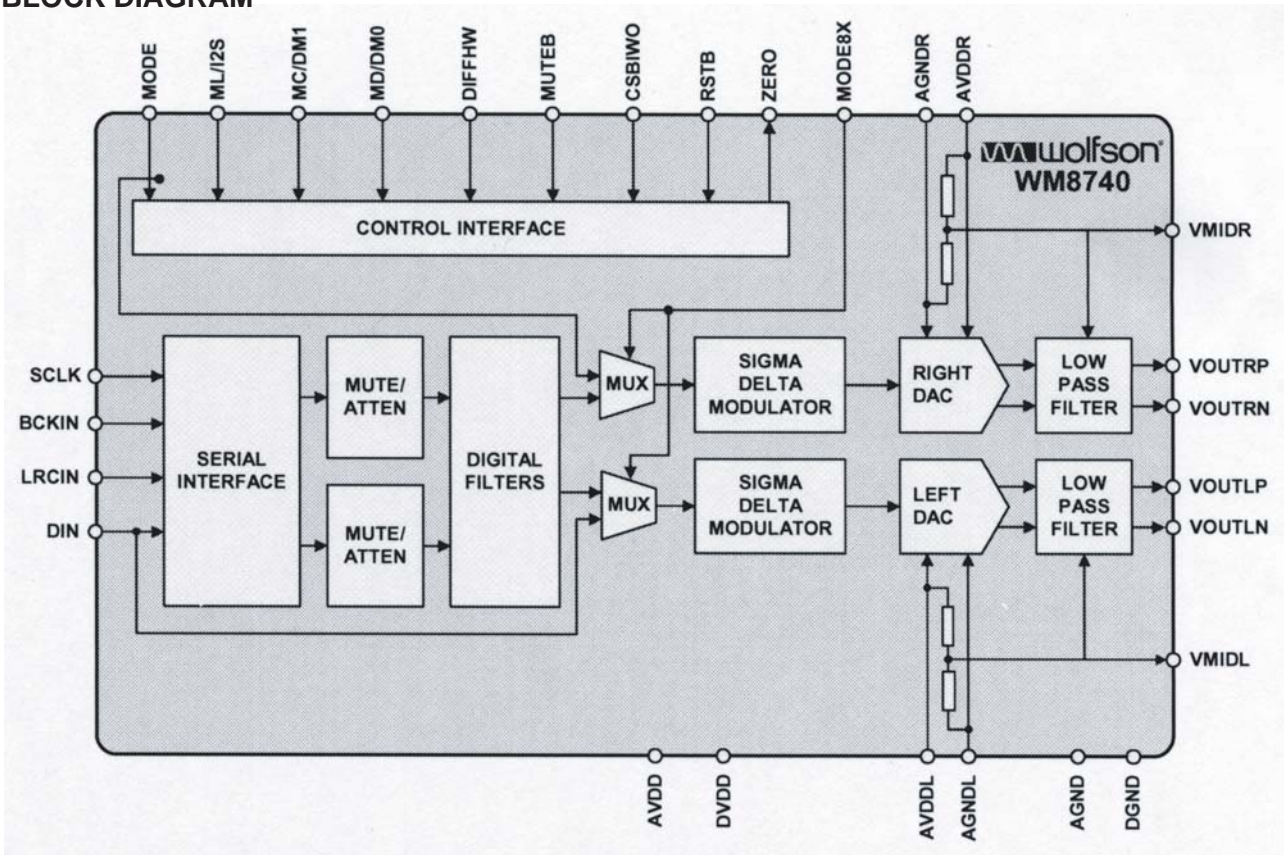
TERMINAL DESCRIPTION (Continued)

Pin No.	Pin name	I/O	Description
88	TEST1	I	Test mode set.
89	DATA	I/O	CPU I/F ARC (DATA).
90	CLOK2	I	CPU I/F ARC (CLK).
91	DVss7	---	Internal digital GND.
92	DVDD7	---	Internal digital power supply.
93	TEST2	I	Test pin. Normally GND.
94	TEST3	I	Test pin. Normally GND.
95	TEST4	O	Open.
96	TEST5	I	Test pin. Normally GND.
97	TEST6	I	Test pin. Normally GND.
98	DVss2	---	Internal digital GND.
99	DVDD2	---	Internal digital power supply.
100	IOVDD2	---	I/O digital power supply.
101	DOUT	O	Digital Out output.
102	TEST	I	Test pin. Normally GND.
103	TES1	I	Test pin. Normally GND.
104	IOVss2	---	I/O digital GND.
105	PLLAVD	---	PLL cell power supply.
106	PLLAVS	---	PLL cell GND.
107	XVss	---	Master clock GND.
108	XTAO	O	Crystal oscillation circuit output.
109	XTAI	I	Crystal oscillation circuit input.
110	XVDD	---	Master clock power supply.
111	AVD4	---	Analog power supply.
112	AOUT1	O	Lch analog output.
113	VREFL	O	Lch reference voltage.
114	AVS4	---	Analog GND.
115	AVS5	---	Analog GND.
116	VREFR	O	Rch reference voltage.
117	AOUT2	O	Rch analog output.
118	AVD5	---	Analog power supply.
119	IOVDD3	---	I/O digital power supply.
120	IOVss3	---	I/O digital GND.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-6

Q4001 : WM8740 (24-BIT DAC) -1/2

BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-7

Q4001 : WM8740 (24-BIT DAC) -2/2

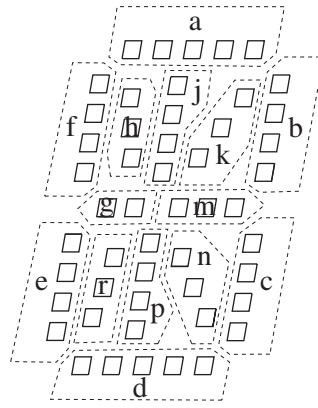
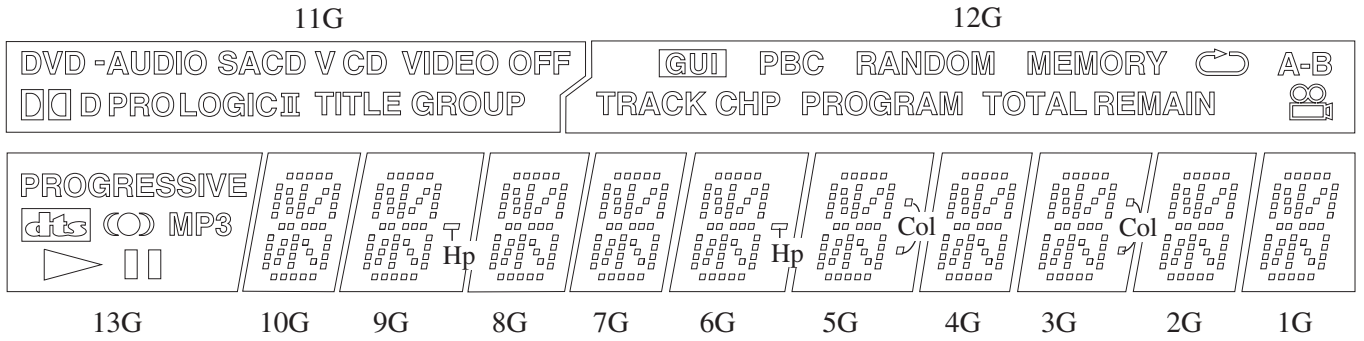
TERMINAL DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital input	Sample rate clock input.
2	DIN	Digital input	Audio data serial input (except in 8XMODE when it is DINL).
3	BCKIN	Digital input	Audio data bit clock input .
4	MODE8X	Digital input	Internal pull-down, active high, 8 x fs mode.
5	SCLK	Digital input	System clock input.
6	DIFFHW	Digital input	Internal pull-down, active high, differential mono mode.
7	DGND	Supply	Digital ground supply.
8	DVDD	Supply	Digital positive supply.
9	AVDDR	Supply	Analogue positive supply.
10	AGNDR	Supply	Analogue ground supply.
11	VMIDR	Analogue output	Mid rail right channel.
12	VOURP	Analogue output	Right channel DAC output positive.
13	VOURN	Analogue output	Right channel DAC output negative.
14	AGND	Supply	Analogue ground supply.
15	AVDD	Supply	Analogue positive supply.
16	VOULN	Analogue output	Left channel DAC output negative.
17	VOULP	Analogue output	Left channel DAC output positive.
18	VMIDL	Analogue output	Mid rail left channel.
19	AGNDL	Supply	Analogue ground supply.
20	AVDDL	Supply	Analogue positive supply.
21	ZERO	Digital output	Infinite zero detect – active low. Open drain type output with active pull-down.
22	RSTB	Digital input	Reset input – active low. Internal pull-up.

PIN	NAME	TYPE	DESCRIPTION			Software Mode
			Normal Mode	Differential Mode	8X Mode	
23	CSBIWO	Digital input Internal pull-down	Wordlength: Low for 16-bit data. High for 20-bit (normal) or 24-bit I ² S data.	Wordlength: Low for 16-bit data. High for 20-bit (normal) or 24-bit I ² S data.	Wordlength: Low for 20-bit data. High for 24-bit data.	Low for serial interface operation.
24	MODE	Digital input Internal pull-up	Low for hardware mode.	Low for left mono mode. High for right mono mode	DINR	High for software mode.
25	MUTEB	Digital input Internal pull-up	Low to soft mute. High for normal operation.	Low to soft mute. High for normal operation.	Low to soft mute. High for normal operation.	Low to soft mute. High for normal operation.
26	MD/DM0	Digital input Internal pull-up	De-emphasis mode select bit 0.	Low for no de-emphasis. High for 44.1kHz de-emphasis.	LRP – LRCLK polarity select.	Control serial interface data signal.
27	MC/DM1	Digital input Internal pull-up	De-emphasis mode select bit 1.	Low for normal filter operation. High for filter slow roll-off.	Unused. Leave unconnected.	Control serial interface clock signal.
28	ML/I2S	Digital input Internal pull-up	Audio serial format: Low – right justified. High – I ² S.	Audio serial format: Low – right justified. High – I ² S.	Input data format: Low – right justified. High – left justified.	Control serial interface load signal.

FL TUBE VIEW

Q8101 : HNV-13SS12T



(1G-10G)

	1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G	13G
P1	a	a	a	a	a	a	a	a	a	a	GROUP	REMAIN	-
P2	h	h	h	h	h	h	h	h	h	h	TITLE	TOTAL	-
P3	l	j	j	j	j	j	j	j	j	j	PRO LOGIC		-
P4	k	k	k	k	k	k	k	k	k	k	D	TRACK	-
P5	b	b	b	b	b	b	b	b	b	b		CHP	-
P6	f	f	f	f	f	f	f	f	f	f	CD	GUI	-
P7	m	m	m	m	m	m	m	m	m	m	V	-B	-
P8	g	g	g	g	g	g	g	g	g	g	SACD	A	-
P9	c	c	c	c	c	c	c	c	c	c	-AUDIO	PROGRAM	-
P10	e	e	e	e	e	e	e	e	e	e	DVD		
P11	r	r	e	r	r	r	r	r	r	r	II	MEMORY	
P12	p	p	p	p	p	p	p	p	p	p	VIDEO OFF	RANDOM	PROGRESSIVE
P13	n	n	n	n	n	n	n	n	n	n	-	PBC	MP3
P14	d	d	d	d	d	d	d	d	d	d	-	-	
P15	-	-	col	-	col	Hp	-	-	Hp	-	-	-	

ADJUSTMENT PROCEDURE

ADJUSTMENT OF MASTER CLOCK FREQUENCY

[When]

1. Exchange super precision clock PC board ass'y (NADG-8725).
2. Exchange IC X001 (Crystal), IC Q9005 (MPC29M33HF), and IC Q8005 (Main microprocessor).

[Procedure]

1. Connect the frequency counter to the test point **P703** on main circuit PC board (NAAR-8645).
2. Press the POWER button to turn on the unit.
3. Wait for 3 minutes. (Heat running)
4. Press and hold down the STOP [■] button, then press the FF (fast forward) [▶▶] button. All segments light up.
5. Press the STOP [■] button, after "NO KEY" is displayed.
6. Press and hold down the PLAY [▶] button, then press the DISPLAY button.

FL display (+ 00)

7. Operate the UP/DOWN (JOG) dial so that the reading of frequency counter becomes **16.934400 MHz +1 / -1 Hz**.

FL display (+ 00)

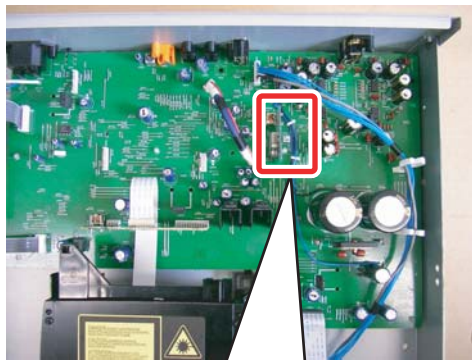
UP dial (JOG) (+ 10) Ex.

DOWN dial (JOG) (- 10) Ex.

8. Press and hold down the DISPLAY button, then press the PUSH TO ENTER (JOG) button.

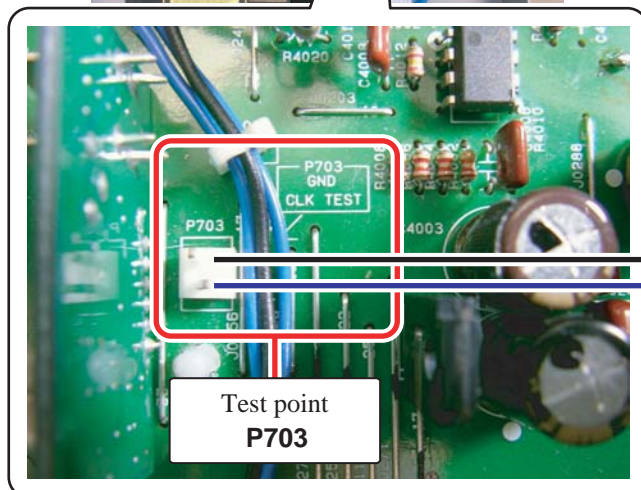
FL display UPDATING.. ---> UPDATE OK

9. Press the PUSH TO ENTER (JOG) button, after "NO DISC" is displayed.
10. Press the POWER button to turn off the unit.
11. Disconnect the frequency counter.

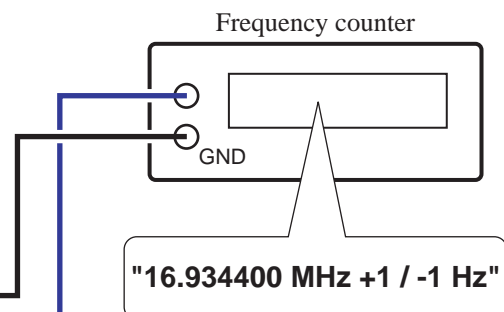


--- Top view ---

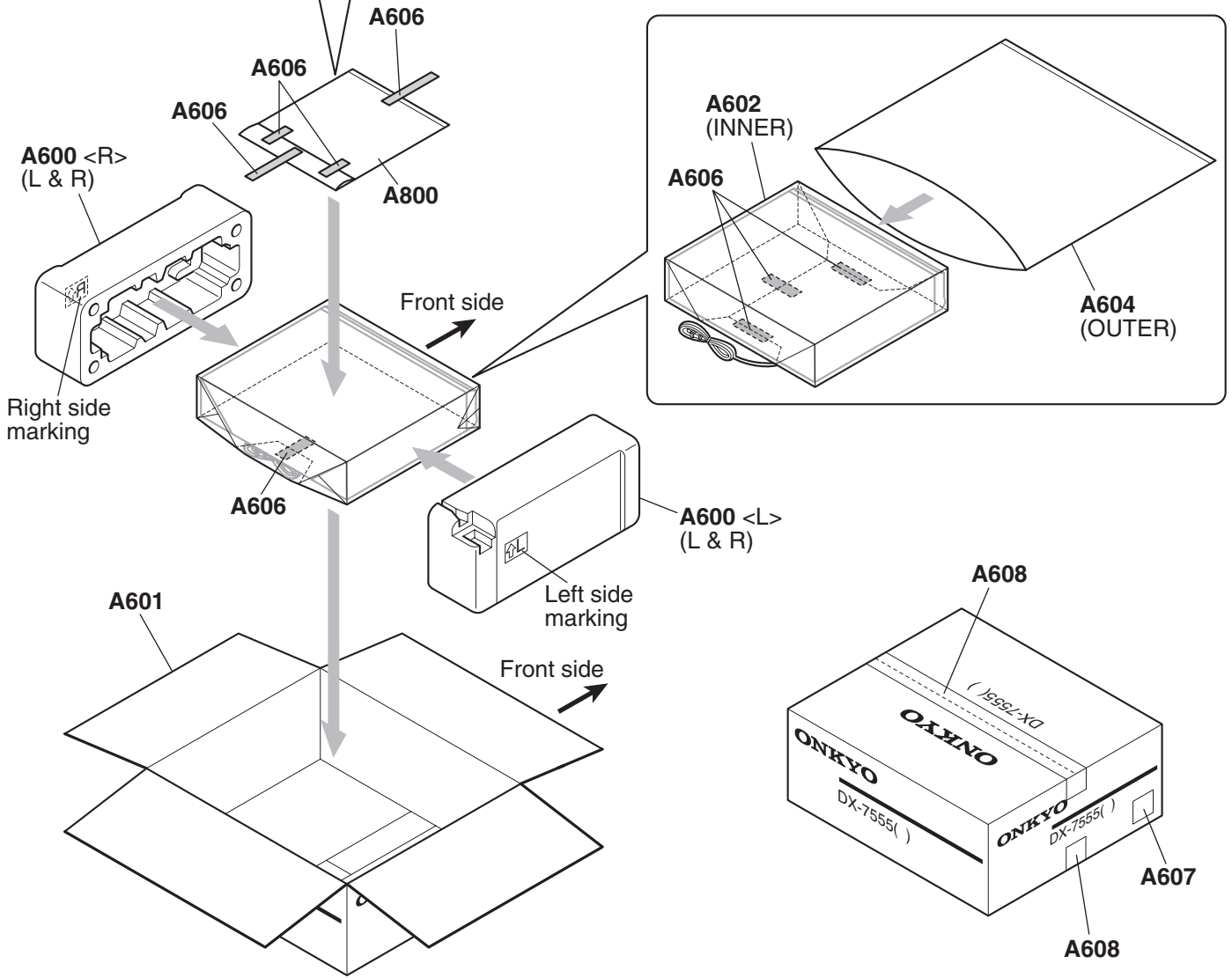
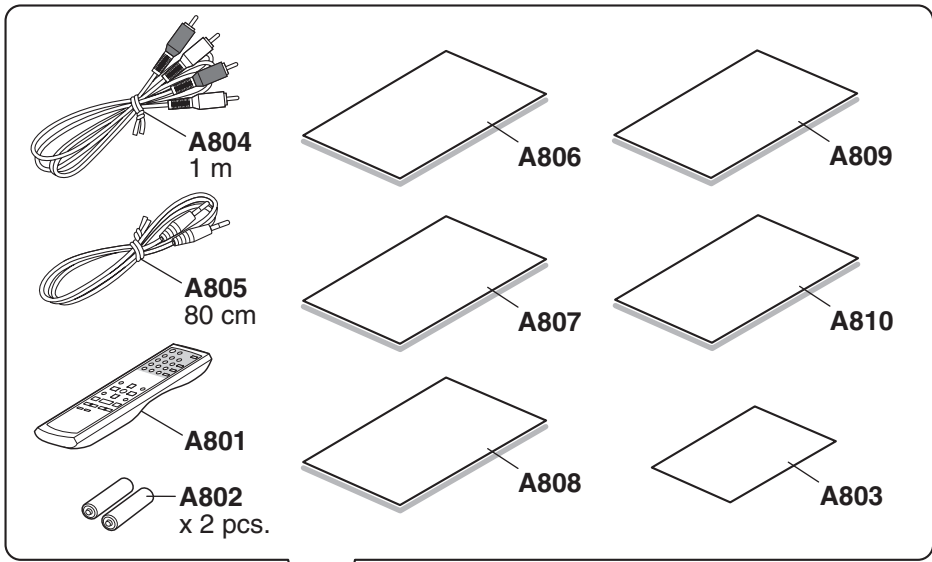
Main circuit PC board (NAAR-8645)



Test point
P703



PACKING PROCEDURE



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